



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,130	02/06/2004	Qadeer A. Khan	SC130241C	8393
23125	7590	07/01/2005	EXAMINER	
FREESCALE SEMICONDUCTOR, INC. LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			NGUYEN, LONG T	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/774,130

Applicant(s)

KHAN ET AL.

Examiner

Long Nguyen

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 May 2005.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6-15 is/are pending in the application.
- 4a) Of the above claim(s) 10-15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 6-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 May 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>5/31/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claims 6-9 are objected to because of the following informalities:

Claim 6, line 40, "power" should be changed to --voltage-- so that the terminology is consistent to avoid unclear antecedent basis.

Claim 6, line 51, "a reference" should be changed to --the reference-- to avoid unclear antecedent basis.

Claims 7 and 8 are objected to because they include the informalities of claim 6.

Claim 9, line 59, "a reference" should be changed to --the reference-- to avoid unclear antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 2-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ng et al. (USP 5,877,633) in view of Nguyen et al. (USP 6,842,043).

With respect to claims 6-9, the circuit in Figures 1-2 of the Ng et al. reference discloses a bidirectional level shifter (102, wherein the detail of 102 is shown in Figure 2) for shifting a low voltage digital signal (106, see lines 2-6 of Col. 2) to a high voltage signal (108, see lines 2-6 of Col. 2), and for shifting the high voltage digital signal (108) to the low voltage digital signal

Art Unit: 2816

(106), wherein Figure 2 shows the bidirectional level shifter (102) comprises: a first I/O terminal (200) for sending and receiving the low voltage digital signal (106); a second I/O terminal (202) for sending and receiving the high voltage digital signal (108); a first circuit (213) coupled to the first and second I/O terminals (200 and 202) wherein the first circuit (213) operates at a low power supply voltage (because circuit 213 is used for shifting a high voltage signal 202 into a low voltage signal 200, so circuit 213 must operate at the low power supply voltage); and a second circuit (212) coupled to the first and second I/O terminals (200 and 202) wherein the first circuit (212) operates at a high power supply voltage (because circuit 212 is used for shifting a low voltage signal 200 into a high voltage signal 202, so circuit 212 must operate at the high power supply voltage). The circuit in Figure 1-2 of the Ng reference does not disclose that the detail of each of the first and second circuits comprising two PMOS transistors, two NMOS transistors and an inverter connected as recited in claims 2 and 4. However, Figure 3 of the Nguyen et al. reference discloses a unidirectional shifter that has an advantage of faster switching and thus the speed of the circuitry is faster (see lines 30-35 of Col. 8 of Nguyen et al.). Therefore, it would have been obvious to one having skills in the art at the time the inventions was made to modify the bidirectional level shifter circuit in Figure 2 of the Ng et al. reference by specifically using the unidirectional level shifter (Figure 3 of Nguyen et al.) for each of the first (213) and second (212) circuits in Figure 2 of the Ng et al. reference for the purpose of improving the speed of the bidirectional level shifter. Thus, this combination/modification meets all the limitations of claims 6-9. Note that, the first circuit (i.e., Figure 3 of Nguyen et al. which replaces circuit block 213 in Figure 2 of Ng et al.) comprising: a first PMOS transistor (P1), a second PMOS transistor (P2), a first NMOS (N1), a second NMOS (N2), a first inverter (P3,

Art Unit: 2816

N3), a fifth PMOS transistor (P5), a fifth NMOS transistor (N5), output (OUT) in Figure 3 of Nguyen et al. is connected to node 200 in Figure 2 of Ng et al. (because output of first circuit 213 connected to node 200 in Figure 2 of Ng et al.), input (IN) in Figure 3 of Nguyen et al. is connected to node 202 in Figure 2 of the Ng et al. (because input of the first circuit 213 is connected to 202 in Figure 2 of Ng et al.), reference voltage (ground), and power supply voltage (Hi-V) in Figure 3 of Nguyen et al. in this case is changed to be the low supply voltage Lo-V since the circuit 213 must be operated by the low voltage to shift the signal from the high voltage into the low voltage, and voltage (Lo-V) for inverter (P3, N3) must be changed to Hi-V since the input of the first circuit 213 receives the signal at a high voltage level to shift into the low voltage level at the output of 213. Also note that, the second circuit (i.e., Figure 3 of Nguyen et al. which replaces circuit block 212 in Figure 2 of Ng et al.) comprising: a third PMOS transistor (P1), a fourth PMOS transistor (P2), a third NMOS (N1), a fourth NMOS (N2), a second inverter (P3, N3), a sixth PMOS transistor (P5) and a sixth NMOS transistor (N5), output (OUT) in Figure 3 of Nguyen et al. is connected to node 202 in Figure 2 of Ng et al. (because output of first circuit 212 connected to node 202 in Figure 2 of Ng et al.), input (IN) in Figure 3 of Nguyen et al. is connected to node 200 in Figure 2 of the Ng et al. (because input of the first circuit 212 is connected to 200 in Figure 2 of Ng et al.), reference voltage (ground) and power supply voltage (Hi-V in Figure 3 of Nguyen et al. in this case is the high supply voltage since the circuit 212 must be operated by the high voltage to shift the signal from the low voltage into the high voltage).

Response to Arguments

4. Applicant's arguments filed on 5/31/05 have been fully considered but they are not persuasive.

In response to applicant's arguments against the references (Ng and Nguyen) individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant also argues that the combining the teaching of Ng and Nguyen may provide a bidirectional level shifter would includes a plurality of pull-up resistors, and would thus constantly consumes DC current, and since the present invention does not include any pull-up resistors, it consumes less current. However, this argument is not persuasive because claims 6-9 does not recite any specific recitation to exclude the pull-up resistors in the bidirectional shifter system, so the combination as discussed meets all the limitations of claims 6-9 regardless, whether or not, the pull-up resistors present in the bidirectional shifter system.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. This application contains claims 10-15 drawn to an invention nonelected with traverse in the non-final office action. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2816

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 27, 2005


LONG NGUYEN
PRIMARY EXAMINER